Abstract of the Disclosure:

In a semiconductor integrated circuit device, a command decoder 8 is adapted to receive not only an external command but also an internal command. An ECC controller 6 has a command generator and an address generator. When the command decoder 8 decodes an external entry command, the command generator instructs encoding to an ECC-CODEC circuit 7 and the address generator sequentially produces addresses which are supplied to a memory array. The ECC-CODEC circuit 7 produces check bits for error detection/correction with reference to information data of the memory array. Upon completion an encoding operation of writing the check bits into a predetermined region of the memory array, the ECC controller 6 delivers an end signal to the command decoder as the internal command to make a super self-refresh control circuit 9 start a super self-refresh operation.